CLAIMS

1. A method for processing variable width instructions in a pipelined processor, comprising:

decoding instructions to identify a loop setup instruction having a loop setup instruction address and containing a loop bottom offset;

decoding instructions following the loop setup instruction, each having an instruction address and containing an instruction width; and

for each instruction following the loop setup instruction, using a current instruction address, a current instruction width, the loop setup instruction address and the loop bottom offset to determine if the next instruction is a loop bottom instruction.

2. A method as defined in claim 1, wherein determining if the next instruction is a loop bottom instruction comprises determining if the current instruction address plus the current instruction width minus the loop setup instruction address minus the loop bottom offset is equal to zero.

3. A method as defined in claim 1, wherein determining if the next instruction is a loop bottom instruction comprises determining if the current instruction address plus the current instruction width plus the loop setup instruction address inverted plus the loop bottom offset inverted plus 1 is equal to negative 1.

4. A method as defined in claim 3, wherein the step of determining if the next instruction is a loop bottom instruction is performed by a plurality of adders, a plurality of exclusive OR gates receiving outputs of the adders and an AND gate receiving outputs of the exclusive OR gates.

5. A method as defined in claim 1, further comprising identifying a next instruction following the loop setup instruction as a loop bottom instruction if the loop bottom offset is equal to a width of the loop setup instruction.

6. Apparatus for processing variable width instructions in a pipeline processor, comprising:

an instruction decoder configured to decode a loop setup instruction, having a loop setup instruction address, to obtain a loop bottom offset and configured to decode instructions following the loop setup instruction, each having an instruction address, to obtain an instruction width;

registers for holding the loop setup instruction address and the loop bottom offset; and

a loop bottom detector, responsive to a current instruction address, a current instruction width, the loop setup instruction address and the loop bottom offset, configured to determine if a next instruction is a loop bottom instruction.

7. Apparatus as defined in claim 6, wherein the loop bottom detector is configured to determine if the current instruction address plus the current instruction width plus the loop setup instruction address inverted plus the loop bottom offset inverted plus one is equal to negative one.

8. Apparatus as defined in claim 7, wherein the loop bottom detector comprises a plurality of adders receiving the current instruction address, the current instruction width, the loop setup instruction address inverted, the loop bottom offset inverted and one, a plurality of exclusive OR gates

receiving outputs of the adders and an AND gate receiving outputs of the exclusive OR gates to provide a loop bottom indication.

9. Apparatus for processing variable width instructions in a pipelined processor, comprising:

means for decoding a loop setup instruction, having a loop setup instruction address, to obtain a loop bottom offset and for decoding instructions following the loop setup instruction, each having an instruction address, to obtain an instruction width;

means for holding the loop setup instruction address and the loop bottom offset; and

means, responsive to a current instruction address, a current instruction width, the loop setup instruction address and the loop bottom offset, for determining if a next instruction is a loop bottom instruction.

10. Apparatus as defined in claim 9, wherein the means for determining if a next instruction is a loop bottom instruction comprises means for determining if the current instruction address plus the current instruction width minus the loop setup instruction address minus the loop bottom offset is equal to zero.

11. Apparatus as defined in claim 9, wherein the means for determining if a next instruction is a loop bottom instruction comprises means for determining if the current instruction address plus the current instruction width plus the loop setup instruction address inverted plus the loop bottom offset inverted plus one is equal to negative 1.

12. Apparatus as defined in claim 11, wherein the means for determining if the next instruction is a loop bottom instruction comprises a plurality of adders, a plurality of exclusive OR gates receiving outputs of the adders and an AND gate receiving outputs of the exclusive OR gates.